STANDARD ATA QUEUING AUTOMATION IN SERIAL ATA INTERFACE

ABSTRACT

A method and circuit for enhancing the performance in a serial ATA interface uses a standard ATA queue automation circuitry that handles all the transmit/receive frame information structure (FIS) operations for ATA queue commands without interrupting the higher-level software and associated hardware, firmware, and drivers. If the standard ATA queue automation circuitry and command queues are not provided, then every FIS operation will interrupt the higher layer application program. The standard ATA queuing automation circuit preprocesses higher layer commands to write into the task file registers before initiating the transport layer for an FIS transmission and provides information regarding the success or failure of a command. Commands to be executed and completion command queues are preferably used to improve the performance further. These queues may be implemented within the higher layers, as part of the standard ATA queuing automation circuit, or as software, firmware, and/or hardware functionally located between the standard ATA queuing automation circuit and the higher layers. The standard ATA queue automation circuitry provides information to program the DMA controller and activates the DMA automatically for the data transfer.